PhD-microelectronic
New methodologies for analysis of metal-dielectric interfaces for high integrated passive devices from 2D to 3D

Practical information

Recommended training:
Master 2 or Engineering school in microelectronic, physic or science

University: Normandie Université Caen

Desired start date of the thesis: 01-10-2023

Duration: 3 years

Establishment / Location:
CRISMAT Campus 2 Caen

Thesis Director: R. Coq Germanicus CRISMAT Laboratory 6 Bv Marechal Juin Bat G 14000 Caen

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How to candidate:
by e-mail with a CV and motivation letter
In French or English

In the French CNRS research lab CRISMAT, based in Caen Normandy, the joint laboratory IPDN (Integrated Passive Devices in Normandy, build to develop new generations of passive electronic components) brings together researchers involved in accelerating the development of highly, or even extremely, integrated passive technology. The Japanese company Murata has started the industrialization of this technology on its site in CAEN and now qualify the very 3D advanced technology.

Nevertheless, in order to address the optimization and reliability of the 3D microelectronic technology, the search for new methodologies of structural and electrical properties of the metal-dielectric interface is still on. The methodologies are based on experimental and physical simulations of the electrical behavior at the interface of the two materials (metal and dielectric).

Considering the reduced dimensions of the devices and structures, the determination of the structural and electrical properties at the nanoscopic scale is necessary to understand and predict the mechanisms at stake during the manufacturing and during the use of the component. Methodologies require methods adapted to the spatial scales of the components. In the framework of the PhD, the methodology will gather all the activities related to the localization of the area of interest, to the representativeness of the local analysis compared to the globality of the device. The work will start on two-dimensional (2D) structures such as MIM (Metal/Dielectric/Metal) and will extend in a second time to three-dimensional (3D) structures (where the depth of the material is used to multiply the interface surface). In this context, the objectives of the thesis are: (1) the determination of the physical phenomena at the interface of the two materials: conductor and insulator, (2) the scale change from micrometer to nanometer (3) the simulation of the nano-electrical system. For the experimentation, the techniques used will be based on the means available in the laboratory (mainly microscopy) and in the industry (electrical and structural conformity tests, reproducibility...). For simulation, a device simulator will be used.

For applying to this PhD position, the candidate must have a Master 2 or research engineer degree. He/she should have a good knowledge of microelectronics, microelectronic manufacturing processes, electrical and structural characterization and component simulation. Knowledge of Atomic Force Microscopy (AFM) and/or Scanning Electron Microscopy (SEM) techniques can be an advantage.